



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRM/	IN NO.
10/623,082	07/17/2003	Peter A. Burke	02-0279/1D / LSIIP199D1	3302	
24319	7590	06/29/2005			
LSI LOGIC CORPORATION 1621 BARBER LANE MS: D-106 MILPITAS, CA 95035			EXAMINER RICHARDS, N DREW		
			ART UNIT	PAPER NUMBER	
			2815		

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/623,082

Applicant(s)

BURKE ET AL.

Examiner

N. Drew Richards

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 April 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 19-32 is/are pending in the application.
- 4a) Of the above claim(s) 20-22 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 19 and 23-30 is/are rejected.
- 7) ☒ Claim(s) 31 and 32 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 June 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/8/05 has been entered.

Election/Restrictions

2. Claims 20-22 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on October 6, 2004.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 19, 23 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao (USPAT 6198170, Zhao) in view of Colgan et al. (USPAT 5565707, Colgan).

With regard to claim 19, Zhao discloses in figure 4-6 a method for forming an electrical interconnection structure (430) for connection to large electrical contacts (410). Zhao discloses in figures 4 and 5, and column 14 lines 22-28, providing a semiconductor substrate (432/450) having a copper-containing pad layer (422/502) formed thereon such that the copper-containing pad layer includes a plurality of elongate slots (504) having a long axis, a short axis, and sidewalls (adjacent to 504), the slots extending through the pad layer to expose the underlying semiconductor substrate (underlying substrate in contact with 504). Zhao discloses in figure 4 and 6 and column 15 lines 7-24, forming, over the pad layer, a dielectric layer (604) having a plurality of elongate openings (trenches filled by metal 602) formed therein, the elongate openings having a long axis, a short axis, and sidewalls (adjacent 602) and are configured to extend into the dielectric layer to a depth sufficiently deep into the dielectric layer so that electrical connection to the underlying conductive pad layer can be formed. It is not clear if Zhao teaches exposing a "substantial" portion of the sidewalls of the pad layer. Colgan teaches in figure 2 exposing a "substantial" portion of a sidewall of an underlying feature (30/47) while etching an insulating layer (34). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the exposing a portion of the sidewall of Colgan in the method of Zhao in order to increase the contact area of an overlying feature and therefore increase current flow through the finished pad structure of Zhao. Zhao discloses in figures 4 and 6 and column 15 lines 7-24, forming elongate copper-containing contacts (602) in the plurality of openings thereby establishing electrical connections to the underlying copper-

Art Unit: 2815

containing pad layer. In the combination of references, it is obvious that the elongate copper-containing pads would physically contact the exposed portions of the sidewalls since they are formed entirely filling the elongate openings. Zhao discloses in figures 4 and 7-11 conducting further processing as needed.

With regard to claim 23, Zhao teach in figure 4-6 and column 15 lines 7-24, wherein the step of forming the dielectric layer comprises forming the dielectric layer such that the long axis of the elongate openings lie transverse to the long axis of the elongate slots. In the combination, it has already been shown that the substantial portions of the sidewalls will be exposed.

With regard to claim 26, Zhao discloses in figures 4 – 6 a method for forming an electrical interconnection structure (430) for connection to large electrical contacts (410). Zhao discloses in figures 4 and 5, and column 14, lines 22 – 28 providing a semiconductor substrate (432/450) having a conductive pad layer formed thereon such that the copper-containing pad layer (422/502) includes a plurality of elongate slots (504) having a long axis, a short axis, and sidewalls (adjacent to 504), the slots extending through the pad layer to expose the underlying semiconductor substrate (underlying substrate in contact with 504). Zhao discloses in figures 4 and 6, and column 15, lines 7 – 24 forming a dielectric layer (604) over the pad layer. Zhao discloses in figures 4 and 6 and column 15, lines 7 – 24 forming a plurality of elongate trenches (trenches filled by metal 602) in the dielectric layer, the elongate trenches having a long axis, a short axis, and sidewalls (adjacent 602) and are configured such that the long axis of the elongate trenches lies transverse to the long axis of the

Art Unit: 2815

elongate slots in the pad layer to expose a portion of the pad layer wherein the trenches extend sufficiently deep into the dielectric layer so that electrical connections to the underlying conductive pad layer can be formed. It is not clear if Zhao teaches exposing a portion of the sidewalls of the pad layer. Colgan teaches in figure 2 exposing a portion of a sidewall of an underlying feature (30/47) while etching an insulating layer (34). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the exposing a portion of a sidewall of Colgan in the method of Zhao in order to increase the contact area of an overlying feature, and therefore increase current flow through the finished pad structure of Zhao. Zhao discloses in figures 4 and 6, and column 15, lines 7 – 24 filling elongate trenches (602) of the dielectric layer with a conductive material to form conductive contacts which form electrical contacts with the tops of the conductive pad, thereby establishing electrical connection to the underlying conductive pad layer. It would have been further obvious in the method of Zhao and Colgan that electrical contacts are formed with the portions of the sidewalls.

5. Claims 24, 25, and 27 – 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao and Colgan as applied to claims 19, 23 and 26 above, and further in view of Simpson (USPAT 6197688).

With regard to claims 24 and 27, Zhao discloses in figures 4 – 6, and column 15, lines 7 – 24 wherein the step of forming elongate copper-containing contacts in the plurality of elongate trenches includes forming a bulk copper containing layer in the

Art Unit: 2815

elongate slots. It is not clear if Zhao discloses forming at least one barrier layer in the elongate slots and forming a seed layer in the elongate slots. Simpson teaches in figures 7 and 8 forming at least one barrier layer (52) and forming a seed layer (54). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the barrier and seed layers of Simpson in the elongate slots in the method of Zhao and Colgan in order to prevent diffusion of copper into the dielectric and other parts of the device, and in order to form the copper layer evenly. Zhao discloses in figures 4 – 6 and column 15, lines 7 – 24 wherein the step of conducting further processing includes removing excess copper-containing materials from a surface of the dielectric layer and electrically connecting the elongate copper-containing contacts to other circuit elements.

With regard to claim 28, Zhao discloses in figure 4 further including the operation of conducting further processing as needed.

With regard to claim 25 and 29, Zhao discloses in figures 4 – 6 wherein the step of conducting further processing includes forming other semiconductor circuit structures (418 – 410).

With regard to claim 30, Zhao discloses in figure 4 wherein the operation of conducting further processing includes forming an electrically conductive top pad (M4) on the dielectric layer wherein the top pad is electrically connected (through V3, M3, V2 and M2) with the conductive contacts.

Allowable Subject Matter

6. Claims 31 and 32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: Prior art of record fails to teach, disclose, or suggest, either alone or in combination forming the elongate openings that expose the sidewalls of the slots in copper-containing pad layer to a depth that extends all the way down to the underlying semiconductor substrate.

Response to Arguments

8. Applicant's arguments filed 3/17/05 have been fully considered but they are not persuasive.

With regard to applicant's argument that the "Zhao dielectric D is formed in the openings of the conductive layer only," it should be noted that the rejection does not rely on the dielectric D to teach the claimed dielectric layer. Instead, dielectric 604 is relied upon to teach the claimed subject matter. As shown in figure 6 of Zhao, and in layer 420 of figure 4, dielectric 604 is "over" the metal M1/502 as shown in figure 5 of layer 422 of figure 4. While applicant has pointed to one figure of Zhao, a careful review of all of figures 4 – 6 clearly indicate that 604 is over the conductive layer 502. Therefore, applicant's arguments are not persuasive and the rejection is proper.

With regard to applicants argument that the exposed sidewall feature of Colgan is an undesirable overetch artifact exposing a trivial portion of the sidewall as opposed to exposing the "substantial" portion as claimed, it should first be noted that the term "substantial" is a very broad term. In the instant case, the term is being interpreted broadly such that, so long as a noticeable portion of the sidewall is exposed a "substantial" portion is taught. Further, the arguments by the attorney that the overetch is merely an "undesirable overetch" does not constitute factual evidence. The reference itself does not state that the feature is "undesirable" and any argument that it is so is merely supposition by the attorney. A valid motivation for employing this feature has been given in the rejection and thus the combination is considered proper.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2815

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'N. Drew Richards', is written over a horizontal line.

N. Drew Richards
AU 2815